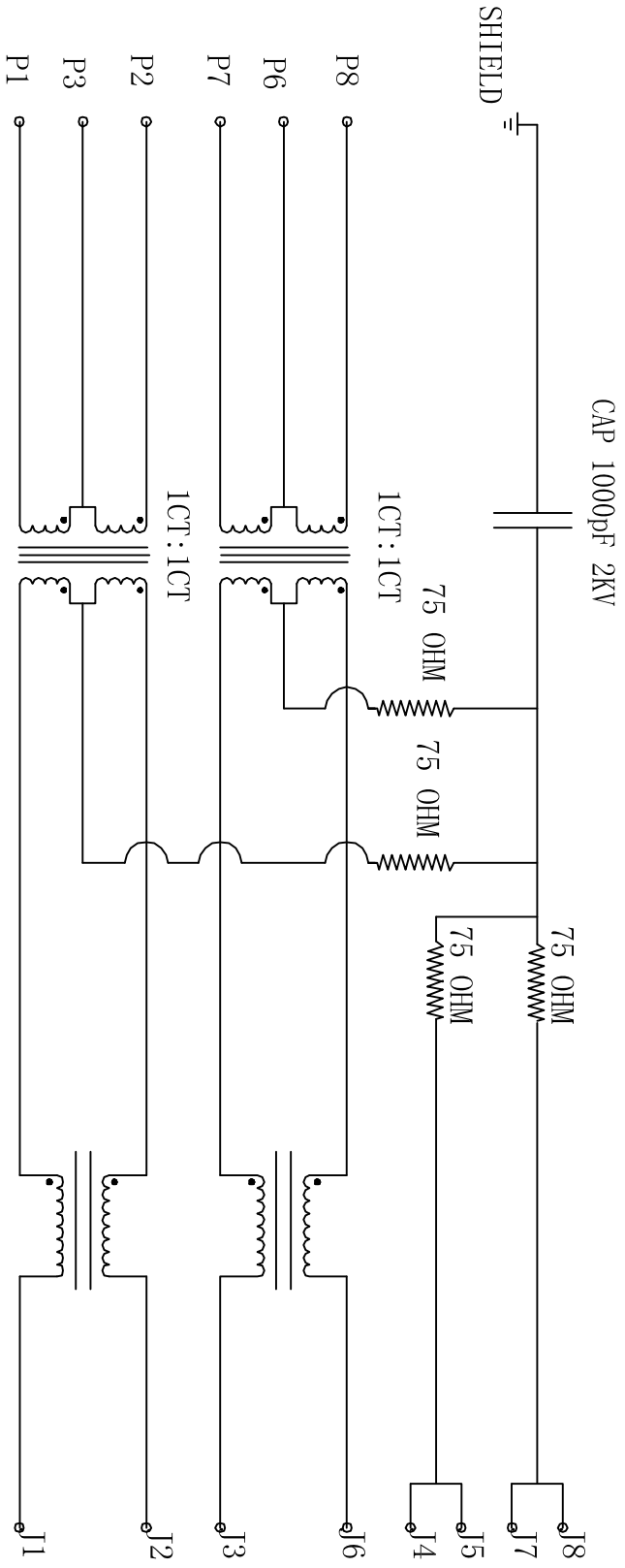


Rev	AWO #	Description	Date	Appr
		SEE SHT 1 OF 2 FOR REVISION		

APPROVED: _____

DATE: _____ TITLE: _____



ELECTRICAL SPECIFICATIONS

- Turns Ratio: (P1 ~ P2) : (J1 ~ J2) 1:1 ±3%
(P7 ~ P8) : (J3 ~ J6) 1:1 ±3%
- Inductance: (P1 ~ P2) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias
(P7 ~ P8) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias
- Leakage Inductance: P1 ~ P2 (with J1 and J2 Short): 0.35uH Max. @ 1 MHz
P7 ~ P8 (with J3 and J6 Short): 0.35uH Max. @ 1 MHz
- Interwinding Capacitor: (P1 ~ P2) : (J1 ~ J2): 1MHz
(P7 ~ P8) : (J3 ~ J6): 35pF max @ 1mhz
- DC Resistance: (J1 ~ J2) : (J3 ~ J6): 1.2 Ohms Max.
- Return Loss: 1MHz to 30MHz: -18dB MIN
30MHz to 60MHz: -(18-20LOG(f/30))dB MIN (WHERE f IS IN MHZ)
60MHz to 80MHz: -12dB MIN
- Dielectric Withstanding: (P1~P2) : (J1~J2): :2250VDC
100KHZ TO 100MHZ : -1.2dB MAX
- Insertion Loss: 100KHZ TO 100MHZ : -1.2dB MAX
- Cross Talk: 1MHZ to 100MHZ: -35dB MIN
- Common to Common mode attenuation: 30KHZ TO 100MHZ: -30dBMIN

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE INCHES [MM]
TOLERANCES: EXCEPT AS NOTED
INCHES HOLES
.X ±.10 Ø.X ±.10
.XX ±.020 Ø.XXX ±.015
.XXX ±.015 Ø.XXX ±.010

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APPROVALS	DATE	TITLE	SIZE	PART NO.	REV.
DRAWN	DY	7/21/10	X	MTJG-4-8TX1-FSD-PG-M35-NRT	-
CHECKED					
APPROVED					