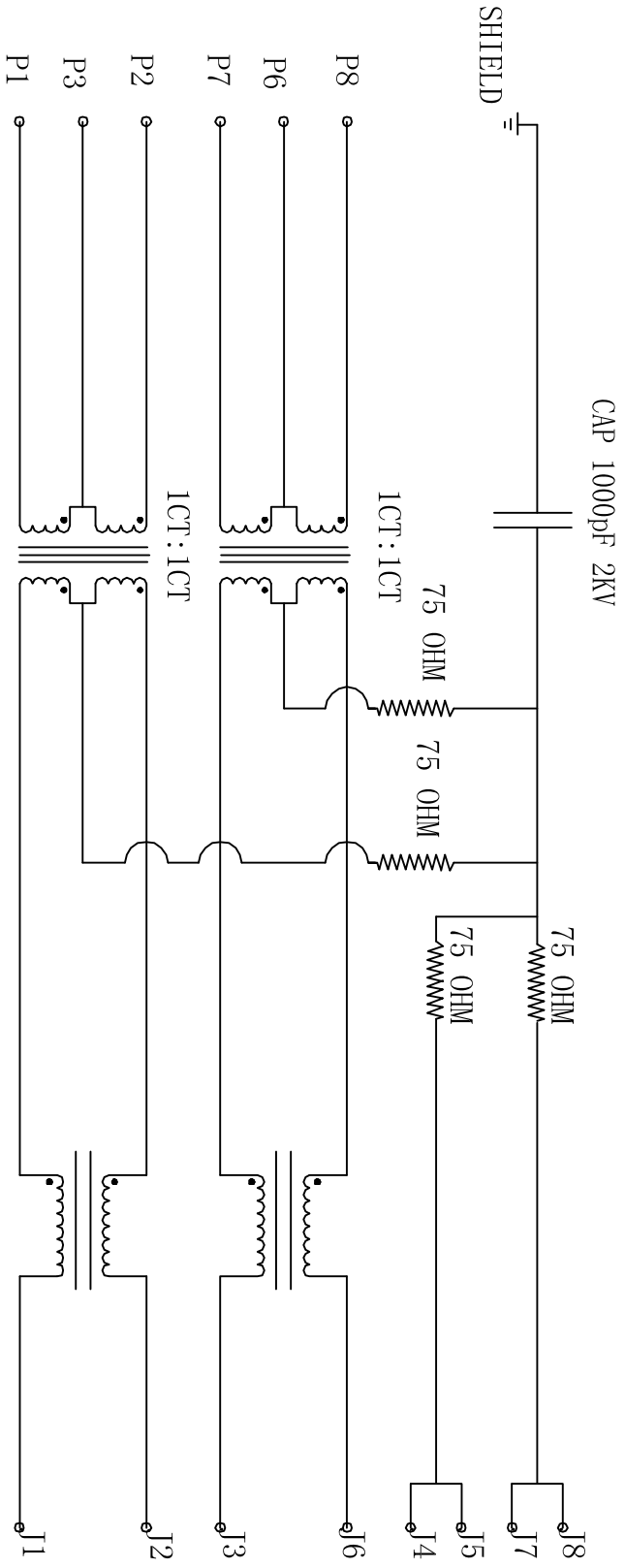


Rev	AWO #	Description	Date	Appr
		SEE SHT 1 OF 2 FOR REVISION		

APPROVED: \_\_\_\_\_

DATE: \_\_\_\_\_ TITLE: \_\_\_\_\_



**ELECTRICAL SPECIFICATIONS**

- Turns Ratio: (P1 ~ P2) : (J1 ~ J2) 1:1 ±3%  
(P7 ~ P8) : (J3 ~ J6) 1:1 ±3%
- Inductance: (P1 ~ P2) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias  
(P7 ~ P8) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias
- Leakage Inductance: P1 ~ P2 (with J1 and J2 Short): 0.35uH Max. @ 1 MHZ  
P7 ~ P8 (with J3 and J6 Short): 0.35uH Max. @ 1 MHZ
- Interwinding Capacitor: (P1 ~ P2) : (J1 ~ J2): 1MHZ  
(P7 ~ P8) : (J3 ~ J6): 35pF max @ 1mhz
- DC Resistance: (J1 ~ J2) : (J3 ~ J6): 1.2 Ohms Max.
- Return Loss: 1MHZ to 30MHZ: -18dB MIN  
30MHZ to 60MHZ: -(18-20LOG(f/30))dB MIN (WHERE f IS IN MHZ)  
60MHZ to 80MHZ: -12dB MIN
- Dielectric Withstanding: (P1~P2) : (J1~J2): (P7~P8) : (J3~J6) : 2250VDC
- Insertion Loss: 100KHZ TO 100MHZ : -1.2dB MAX
- Cross Talk: 1MHZ to 100MHZ: -35dB MIN
- Common to Common mode attenuation: 30KHZ TO 100MHZ: -30dBMIN

UNLESS OTHERWISE SPECIFIED  
ALL DIMENSIONS ARE INCHES [MM]  
TOLERANCES: EXCEPT AS NOTED  
INCHES HOLES  
.X ±.10 Ø.X ±.10  
.XX ±.020 Ø.XXX ±.015  
.XXX ±.015 Ø.XXX ±.010

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TITLE: MODULAR JACK GANGED, 4 PORT, 8P8C

APPROVALS	DATE	SIZE	PART NO.	REV.
DRAWN	DY	7/21/10	MTJG-4-8TX1-FSD-M35-NRT	-
CHECKED				
APPROVED				