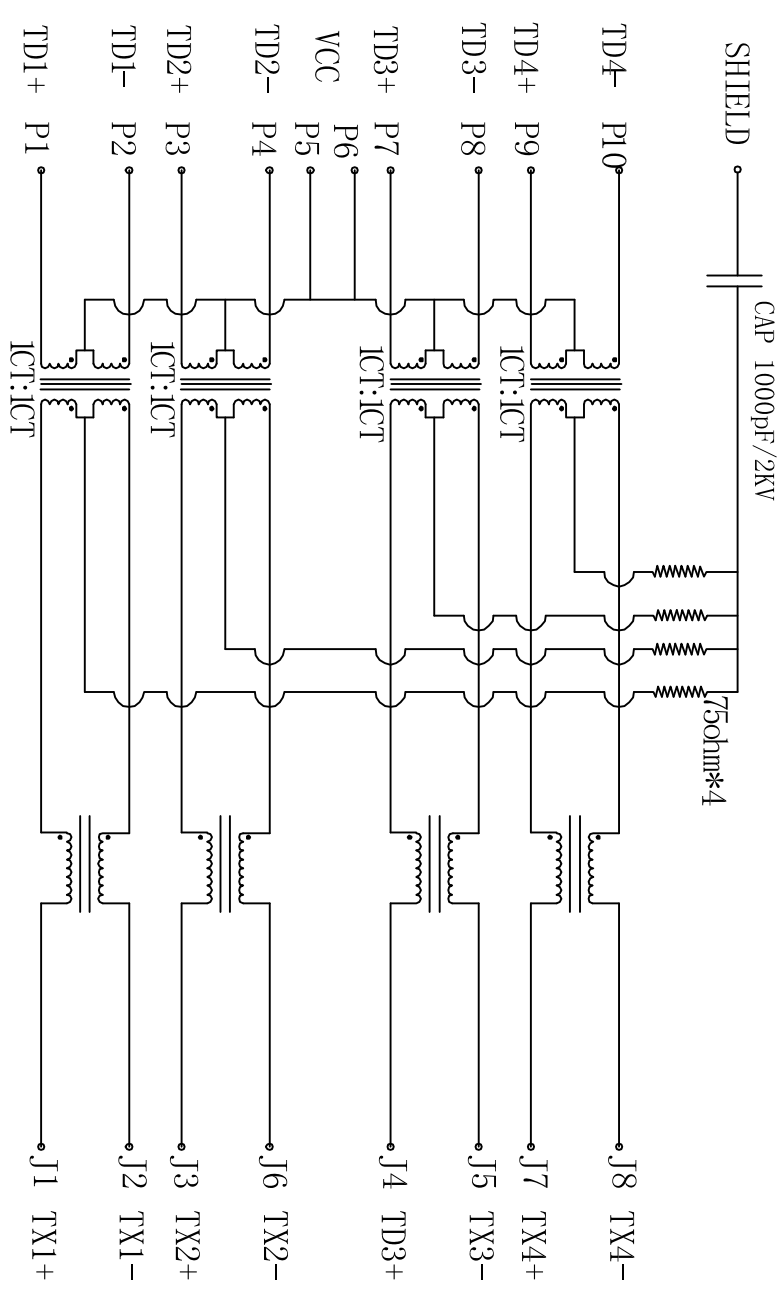


Rev	AWO #	Description	Date	Appr
		SEE SHT 1 OF 2 FOR REVISION		

APPROVED: \_\_\_\_\_

DATE: \_\_\_\_\_ TITLE: \_\_\_\_\_



**ELECTRICAL SPECIFICATIONS**

- Turns Ratio: (P1 ~ P2) : (J1 ~ J2) 1:1 ±3%  
 (P3 ~ P4) : (J3 ~ J6) 1:1 ±3%  
 (P7 ~ P8) : (J4 ~ J5) 1:1 ±3%  
 (P9 ~ P10) : (J7 ~ J8) 1:1 ±3%
- Inductance: (P1 ~ P2) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias  
 (P3 ~ P4) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias  
 (P7 ~ P8) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias  
 (P9 ~ P10) 350uH min. @ 0.1V, 100KHZ, 8mA DC Bias
- Leakage Inductance: P1 ~ P2 (with J1 and J2 Short): 0.3uH Max. @ 1 MHz  
 P3 ~ P4 (with J3 and J6 Short): 0.3uH Max. @ 1 MHz  
 P7 ~ P8 (with J4 and J5 Short): 0.3uH Max. @ 1 MHz  
 P9 ~ P10 (with J7 and J8 Short): 0.3uH Max. @ 1 MHz
- Interwinding Capacitor: (P1 ~ P2) : (J1 ~ J2): 35pF max. @ 1MHz  
 (P3 ~ P4) : (J3 ~ J6): 35pF max @ 1mhz  
 (P7 ~ P8) : (J4 ~ J5): 35pF max @ 1mhz  
 (P9 ~ P10) : (J7 ~ J8): 35pF max @ 1mhz
- DC Resistance: (J1 ~ J2) : (J3 ~ J6): (J7 ~ J8):1.2 Ohms Max.  
 60MHZ to 30MHZ: -19dB min / 30MHZ to 60MHZ: -13dB min
- Return Loss: 1MHZ to 80MHZ: -12dB min / 80MHZ to 100MHZ: -10dB min  
 60MHZ to 80MHZ: -12dB min / 80MHZ to 100MHZ: -10dB min
- Dielectric Withstanding: (P1~P2) : (J1~J2) : (P3~P4) : (J3~J6) :1500V AC  
 (P7~P8) : (J4~J5) : (P9~P10): (J7~J8): 1500V AC
- Insertion Loss: RS=RL=1000HM : 100KHZ TO 80MHZ : -1.1dB Min.  
 OUTPUT VOLTAGE=1V PEAK: 30NS Max  
 PULSE WIDTH=112ns :30NS Max
- Cross Talk: 1MHZ to 100MHZ: 40dB Typ.
- Common to Common mode Attention 30MHZ to 100MHZ: 35dB Typ.

UNLESS OTHERWISE SPECIFIED  
 ALL DIMENSIONS ARE INCHES [MM]  
 TOLERANCES: EXCEPT AS NOTED  
 INCHES HOLES  
 .X ±.10 Ø.X ±.10  
 .XX ±.020 Ø.XXX ±.015  
 .XXX ±.015 Ø.XXX ±.010

**ADAM TECH**  
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TITLE: MODULAR JACK GANGED, 1 PORT, 8P9C

DRAWN	DY	DATE	4/06/10
CHECKED			
APPROVED			
SIZE	PART NO.	REV.	
X	MT-J-88TX1-FSD-M62-P114C	A	
REF:	S00035C	SCALE:	NTS
		SHEET:	2 OF 2